FIG.1

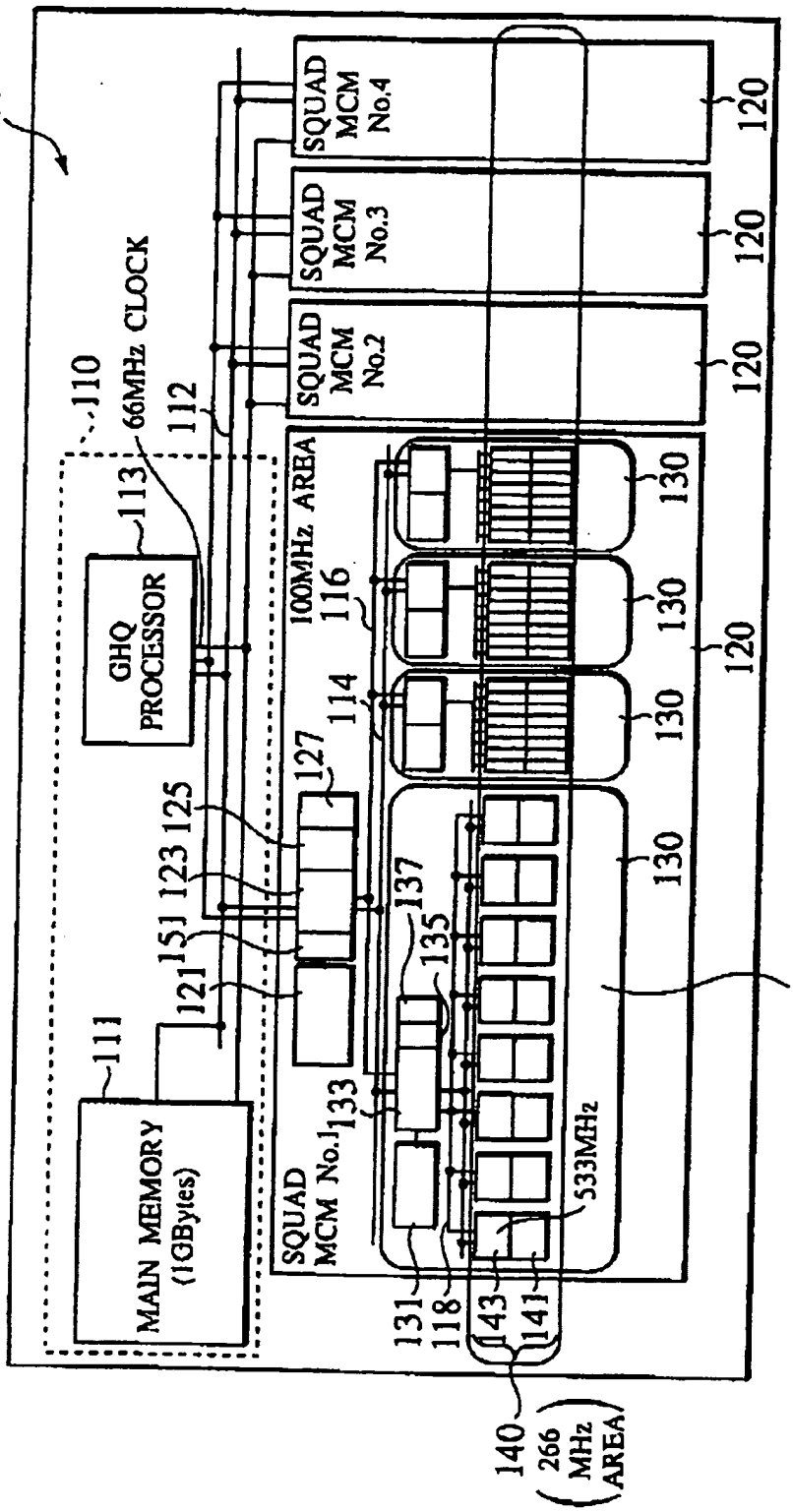

101
110
66MHz CLOCK
112
113
GHQ PROCESSOR
100MHz AREA
116
114
127
125
123
151
121
111
MAIN MEMORY (1GBytes)
SQUAD MCM No.1
133
137
135
131
118
143
141
533MHz
140
266 MHz AREA
SQUAD MCM No.2
SQUAD MCM No.3
SQUAD MCM No.4
120
130
133MHz AREA

FIG.2

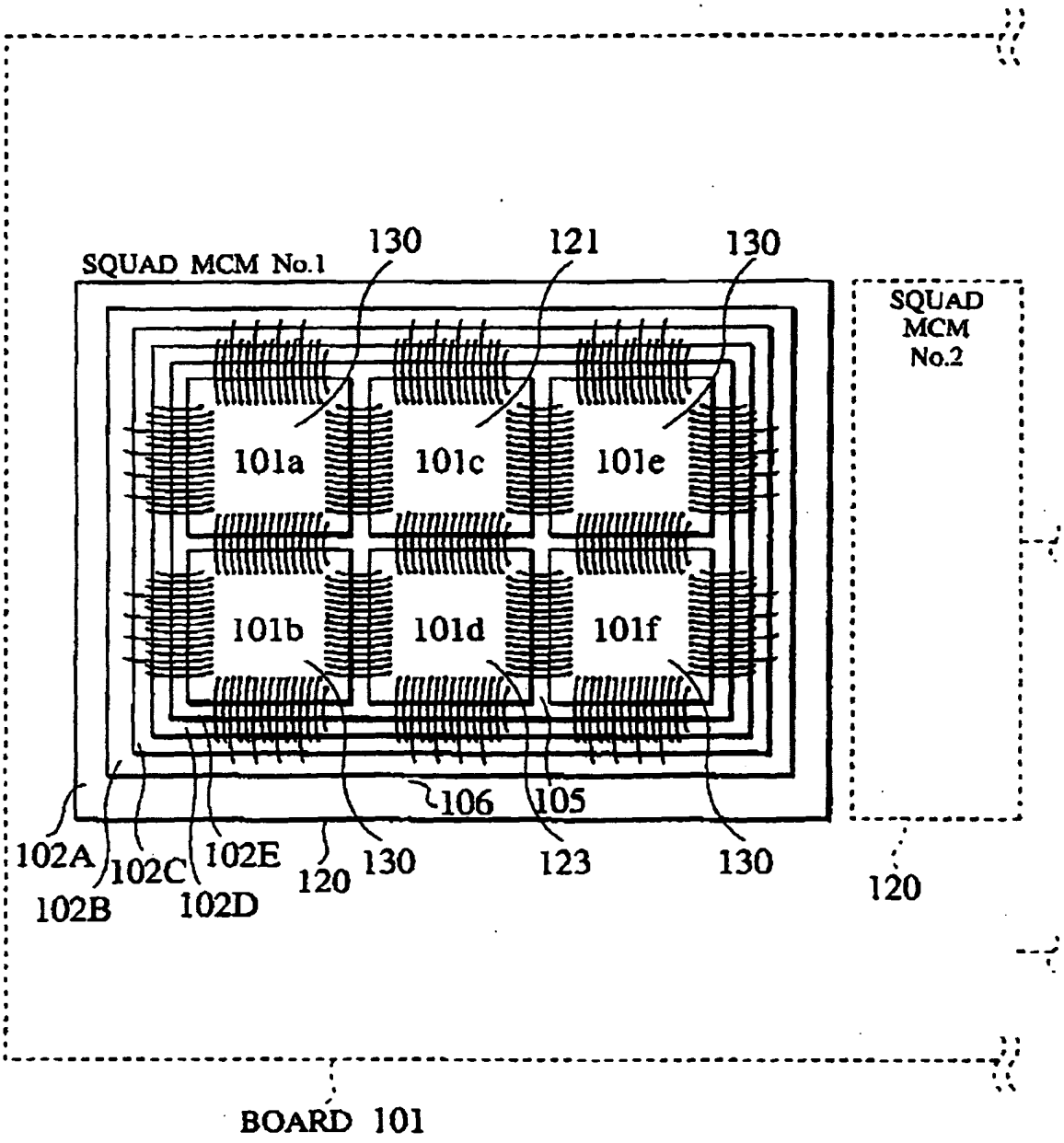

SQUAD MCM No.1
130
121
130
SQUAD MCM No.2
101a
101c
101e
101b
101d
101f
106
105
102A
102B
102C
102D
102E
120
130
123
130
120
BOARD 101

FIG.3

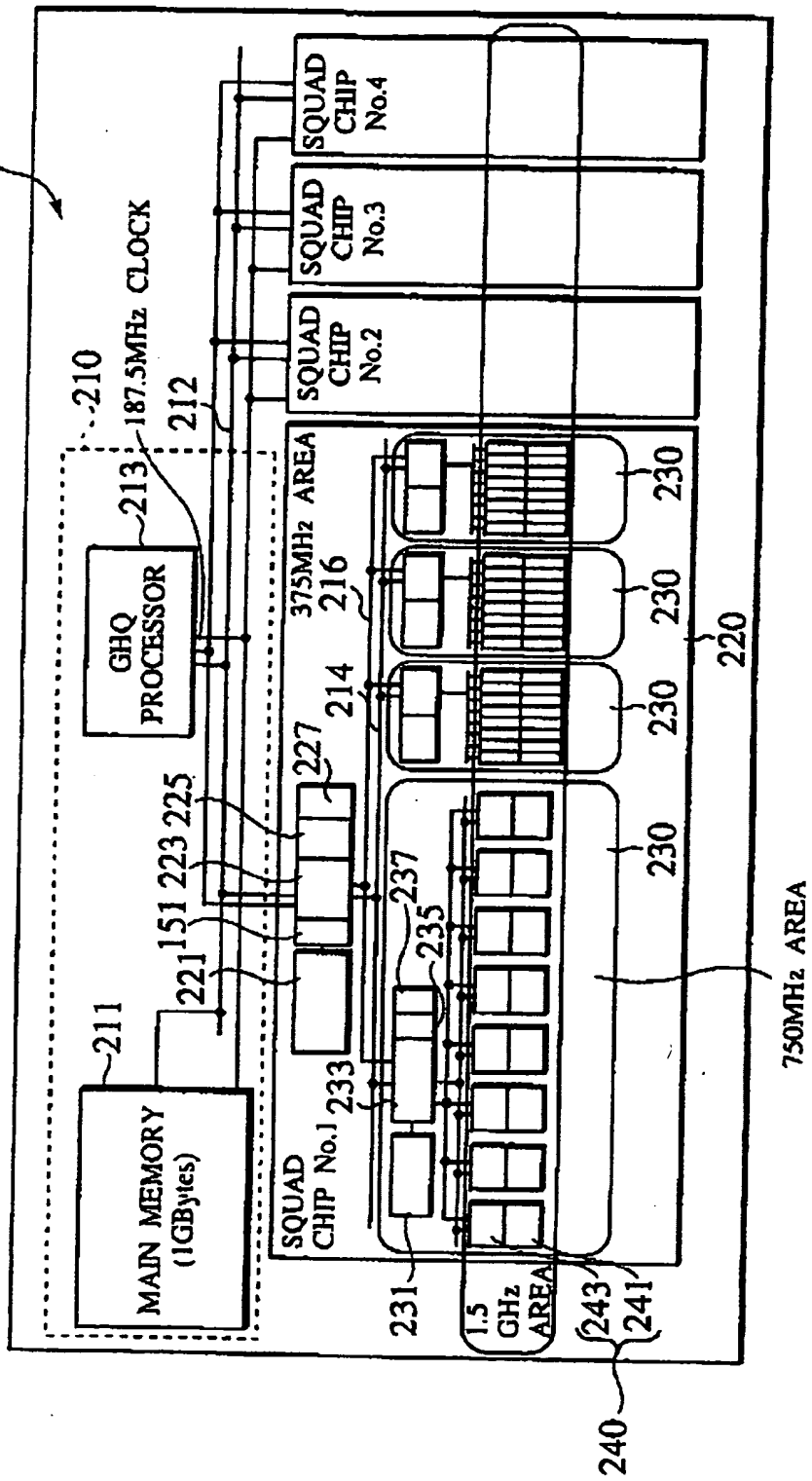

MCM 201
210
187.5MHz CLOCK
212
213
GHQ PROCESSOR
SQUAD CHIP No.4
SQUAD CHIP No.3
SQUAD CHIP No.2
375MHz AREA
216
214
227
225
223
151
221
211
MAIN MEMORY (1GBytes)
SQUAD CHIP No.1
233
237
235
231
1.5 GHz AREA
243
241
240
230
220
750MHz AREA

FIG.4

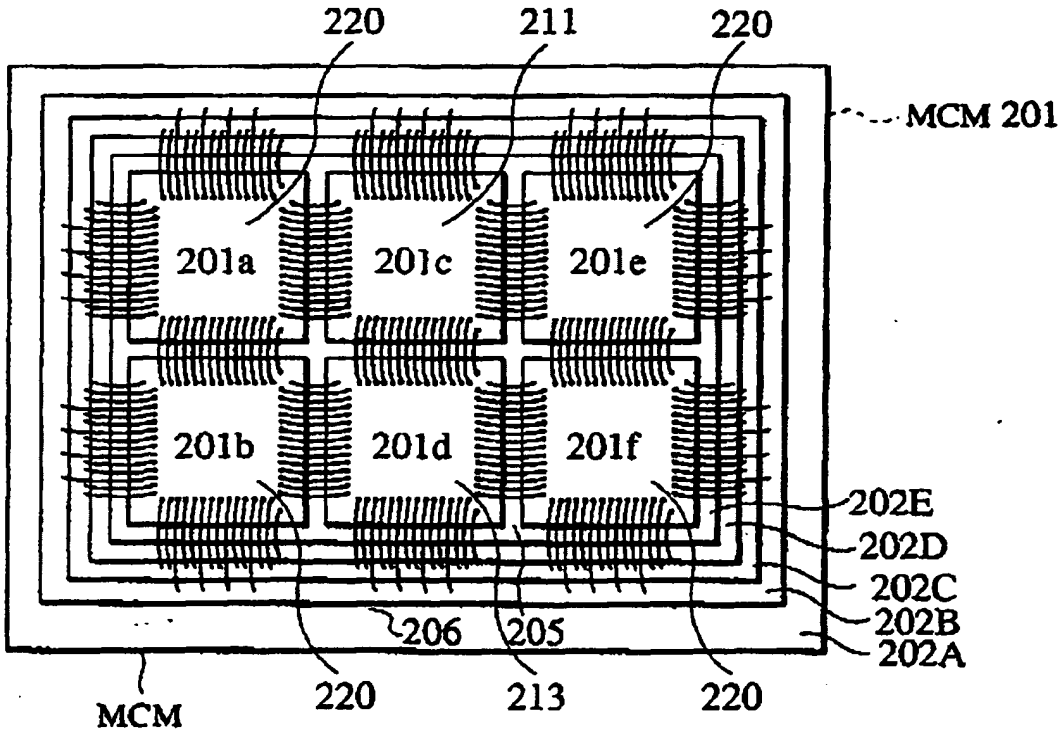

220
211
220
MCM 201
201a
201c
201e
201b
201d
201f
202E
202D
202C
202B
202A
206
205
MCM
220
213
220

FIG.5

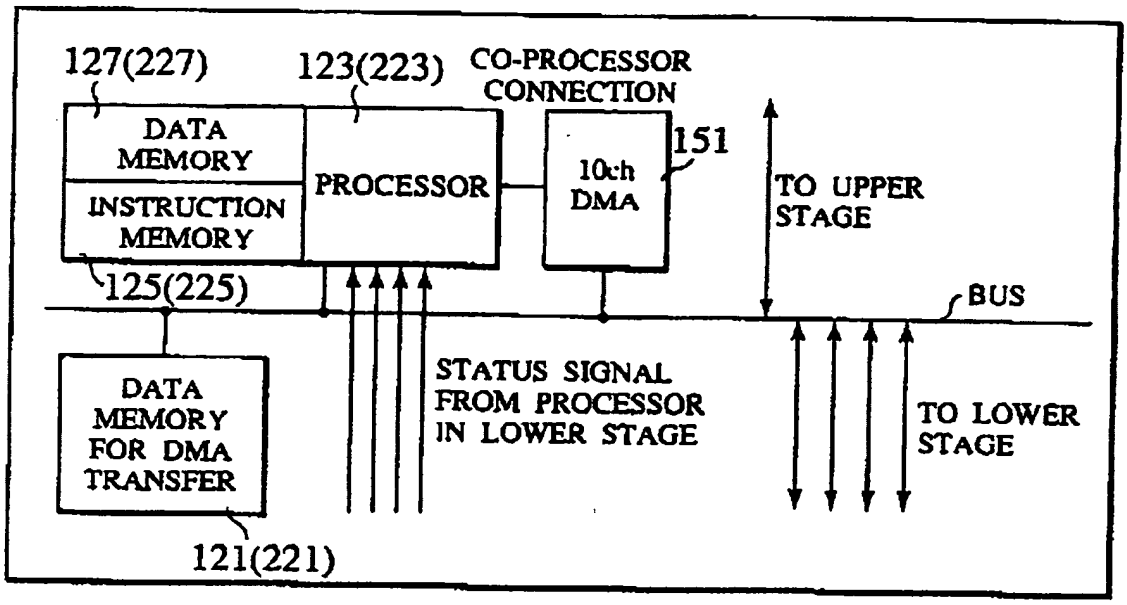

127(227)
123(223)
CO-PROCESSOR CONNECTION
DATA MEMORY
INSTRUCTION MEMORY
PROCESSOR
10ch DMA
151
TO UPPER STAGE
125(225)
BUS
DATA MEMORY FOR DMA TRANSFER
STATUS SIGNAL FROM PROCESSOR IN LOWER STAGE
TO LOWER STAGE
121(221)

FIG.6

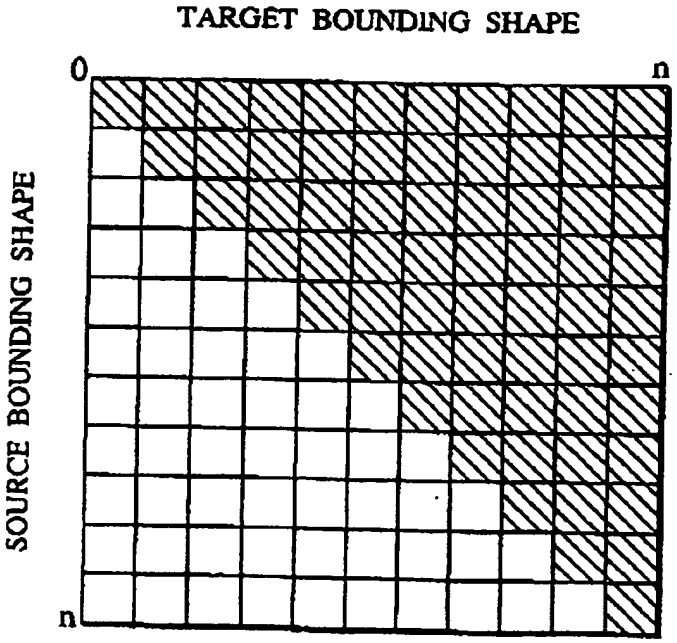

TARGET BOUNDING SHAPE
0
n
SOURCE BOUNDING SHAPE
n

FIG.7

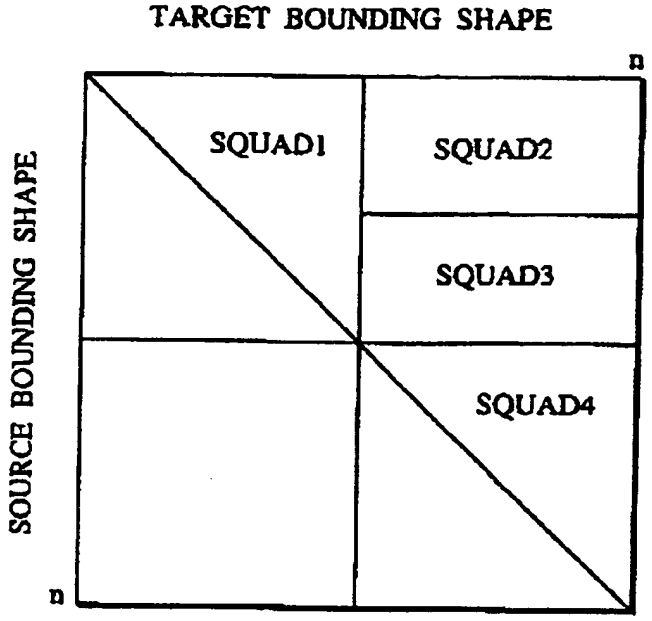

TARGET BOUNDING SHAPE
n
SQUAD1
SQUAD2
SQUAD3
SQUAD4
SOURCE BOUNDING SHAPE
n

FIG.8

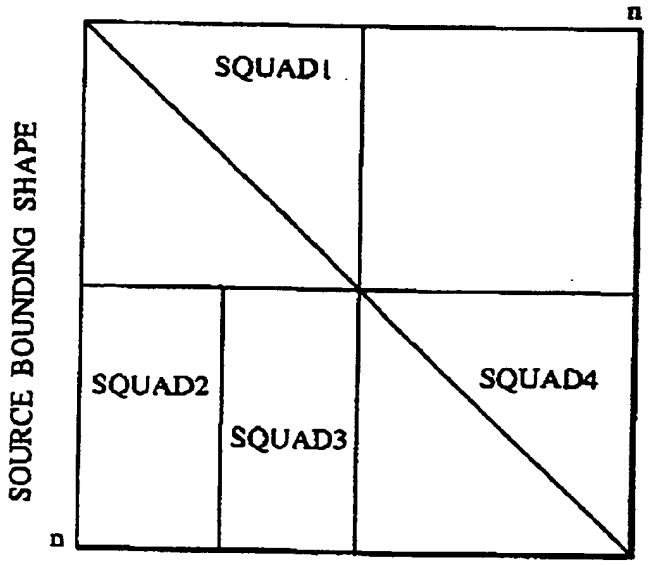
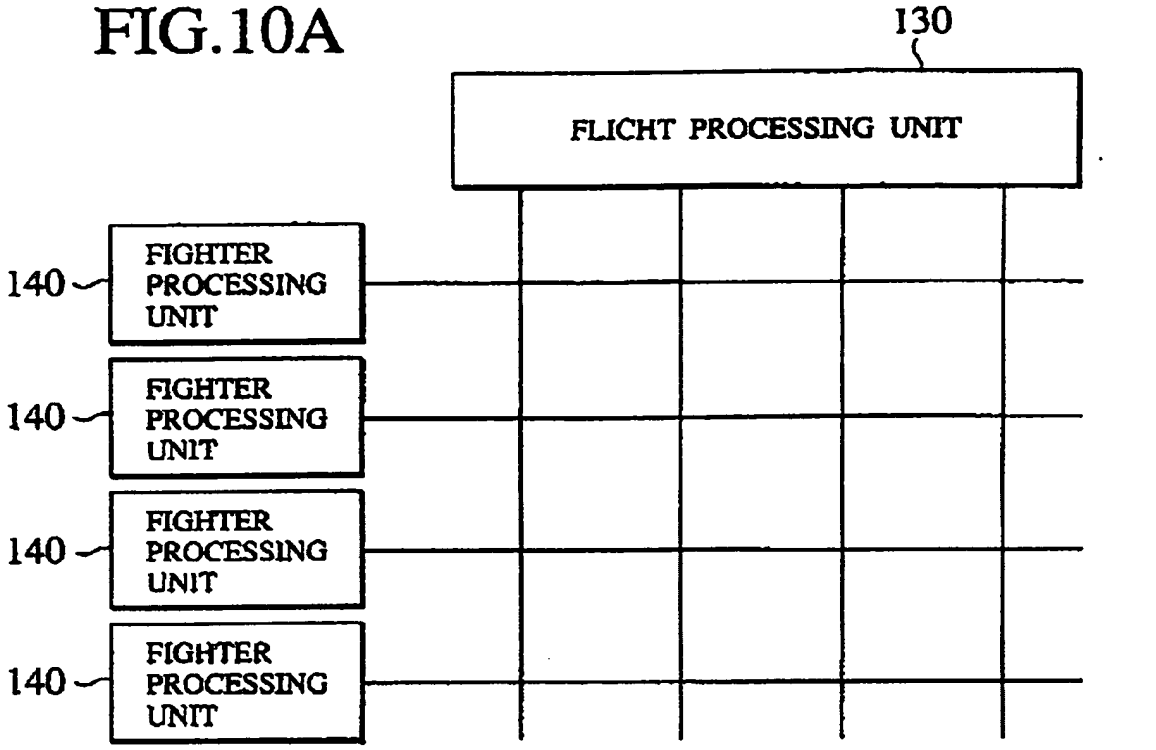

TARGET BOUNDING SHAPE
n
SQUAD1
SQUAD2
SQUAD3
SQUAD4
SOURCE BOUNDING SHAPE
n

FIG.9

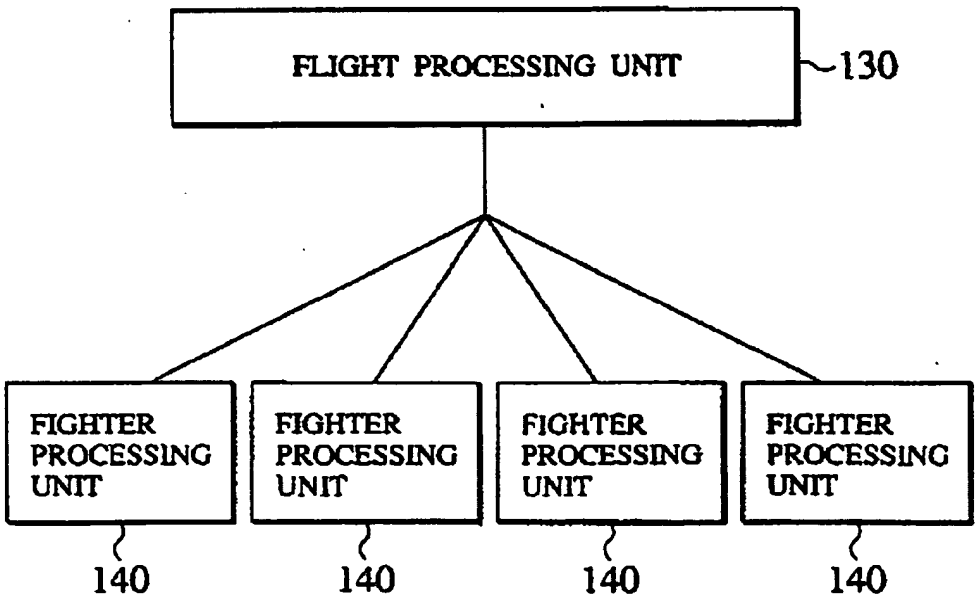
	COLLISION DECISION (PRIOR ART)	COLLISION DECISION (PRESENT INVENTION)
TOTAL PERFORMANCE	COLLISION DECISION IN 69.8G times/sec 50,000 b.s./frame	COLLISION DECISION IN 69.8G times/sec 50,000 b.s./frame
REQUIREMENT FOR MAIN MEMORY SIZE	1.6MBytes	1.6MBytes
REQUIREMENT FOR SQUAD MEMORY SIZE	1.6MBytes	1.6MBytes
REQUIREMENT FOR FLIGHT MEMORY SIZE	0Byte	580KBytes
REQUIREMENT FOR FIGHTER MEMORY SIZE	0Byte	32KBytes
REQUIREMENT FOR BAND WIDTH OF SQUAD BUS	560GBytes/sec	139.2MBytes/sec
REQUIREMENT FOR BAND WIDTH OF FLIGHT BUS	140GBytes/sec	1GBytes/sec

FIG.10A



CROSS-BUS CONNECTION

FIG.10B



STAR CONNECTION